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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/591,683	06/09/2000	Ping-Sheng Tseng	16503-0023	3599

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EXAMINER
LIN, SUN J

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/591,683	Applicant(s) TSENG, PING-SHENG	
	Examiner Sun J Lin	Art Unit 2825	H

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-10 and 15-20* is/are allowed.

6)☒ Claim(s) *1-3 and 11* is/are rejected.

7)☒ Claim(s) *4-7 and 12-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This office action is in response to application 09/591,683 filed on 06/09/2000. Claims 1 – 20 remain pending in the application.

Abstract Objections

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1 – 3 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,425,036 to *Liu et al.* in view of U.S. Patent No. 4,144,448 to *Pisciotta et al.*

5. As to Claim 1, *Liu et al.* show and teach the following subject matters:

- Using electronic design automation (EDA) system to employ *field programmable gate arrays* (*FPGAs*) for *emulating* (i.e., *verifying*) *prototype circuit designs* (i.e., *user circuit designs*)– [title; abstract; Fig. 2];
- FPGAs are debugged by inserting *"read-back" trigger clocks* (i.e., TRIG CLK) in the input – [abstract; Fig. 2]; Trigger-out or read-back is controlled by a user to *trigger asynchronously* a read-back function – [col. 5, line 11 – 14];
- FPGAs are triggered by a plurality of asynchronous clocks – [Fig. 2];
- IOB 269 contains a reception logic for receiving input data to be evaluated – [Fig. 2; col. 6, line 10 – 11];
- *Read-back feature* of FPGAs is employed to debug FPGAs coupled to a *target system* 300 – [abstract; Fig. 2];

Based on the teachings given above, the *EDA* is an *evaluation logic*, and *prototype circuit designs* (*user circuit designs*) in modeled using FPGAs, which are *configurable hardware logic*. Input data to be evaluated within an evaluation time in each FPGA is determined by trigger-out signal controlled by a user.

Liu et al. do not teach using *clock generation logic* for generating a plurality of *asynchronous clocks* by a *master clock* for use by the *evaluation logic* (i.e., FPGAs) and controlling the *phase relationship among the plurality of asynchronous clocks*. But *Pisciotta et al.* show the subject matters in Fig. 1 and teach that a *master clock* is utilized by *Unit 21* (i.e., *clock generation logic*) to produce a plurality of *phase-related clock signals* for *asynchronous validity checking system* – [Fig. 1; title; abstract]. It is obvious that the advantage of using a *master clock* in generating a plurality of phase-related asynchronous clocks for use in the evaluation logic made up of a plurality of

FPGAs is that the duration of evaluation time performed in each FPGA can be accurately controlled.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have utilized the teachings of *Pisciotta et al.* using a master clock in generating a plurality of phase-related asynchronous clocks for accurately controlling the evaluation time of each FPGA in the evaluation logic.

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

6. As to Claim 2, as explained in [Response A] given above, each *FPGA* is *reconfigurable hardware logic*. *Liu et al.* teach that the FPGAs are available commercially from Xilinx, Inc. It is obvious that the FPGA is a *reconfigurable hardware logic chip* available in the market.

For reference purposes, the explanations given above in response to Claim 2 are called **[Response B]** hereinafter.

7. As to Claim 3, reasons are included in **[Response B]** given above.

8. As to Claim 11, reasons are included in **[Response A]** given above.

Allowable Subject Matter

9. Claims 8 – 10 and 15 – 20 are allowed. Claims 4 – 7 and 12 – 14 are objected to as being dependent upon a rejected base claim, but they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Those claims are allowed is because that the prior arts do not teach or suggest the following subject matters:

- *Clock generation logic* includes a plurality of *clock generation slices* and a *clock scheduler* as recited in **[Claims 4 / 5, 6]**;

- A *target system* is controlled by a plurality of *asynchronous clocks* generated by the *clock generation logic* as recited in **[Claim 7]**;
- A *clock generation logic system* for generating a plurality of *asynchronous clocks*, comprising a plurality of *clock generation slices* and a clock *scheduler* as recited in **[Claims 8 / 9, 10]**;
- The method of Claim 11, wherein the step of controlling further comprises steps of: determining a next toggle point from among a plurality of asynchronous clocks from a current time and toggling the clock associated with the next toggle point as recited in – **[Claims 12 / 13, 14]**;
- A method of generating a plurality of asynchronous clocks, where each clock includes a plurality of toggle points and a toggle point represents a point in time where the logic state of the clock changes, comprising steps: determining a first current time, determining a first time duration, comparing, selection and toggling as recited in **[Claims 15 / 16 – 20]**.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J. Lin whose telephone number is (703) 308-4916. The examiner can normally be reached on Monday-Friday (9:00AM-6:00PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703) 308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Sun James Lin
Art Unit 2825
August 25, 2003

VUTHE SIEK
PRIMARY EXAMINER